



Australia 
Austria 
Belgium 
Brazil 
Bulgaria 
Canada
China 
Czech Republic 
Denmark 
Estonia 
Finland 
France 
Germany 
Hungary 
India 
Indonesia 
Ireland 
Israel 
Italy 
Japan 
South Korea 
Latvia 
Lithuania 
Malaysia 
Mexico 
Netherlands 
New Zealand 
Norway 
Poland 
Philippines 
Romania 
Russia 
Serbia 
Singapore 
Slovenia 
South Africa 
Spain 
Sweden 
Switzerland 
Taiwan 
Thailand 
Turkey 
Ukraine 
United Kingdom 
USA 
Việt Nam 



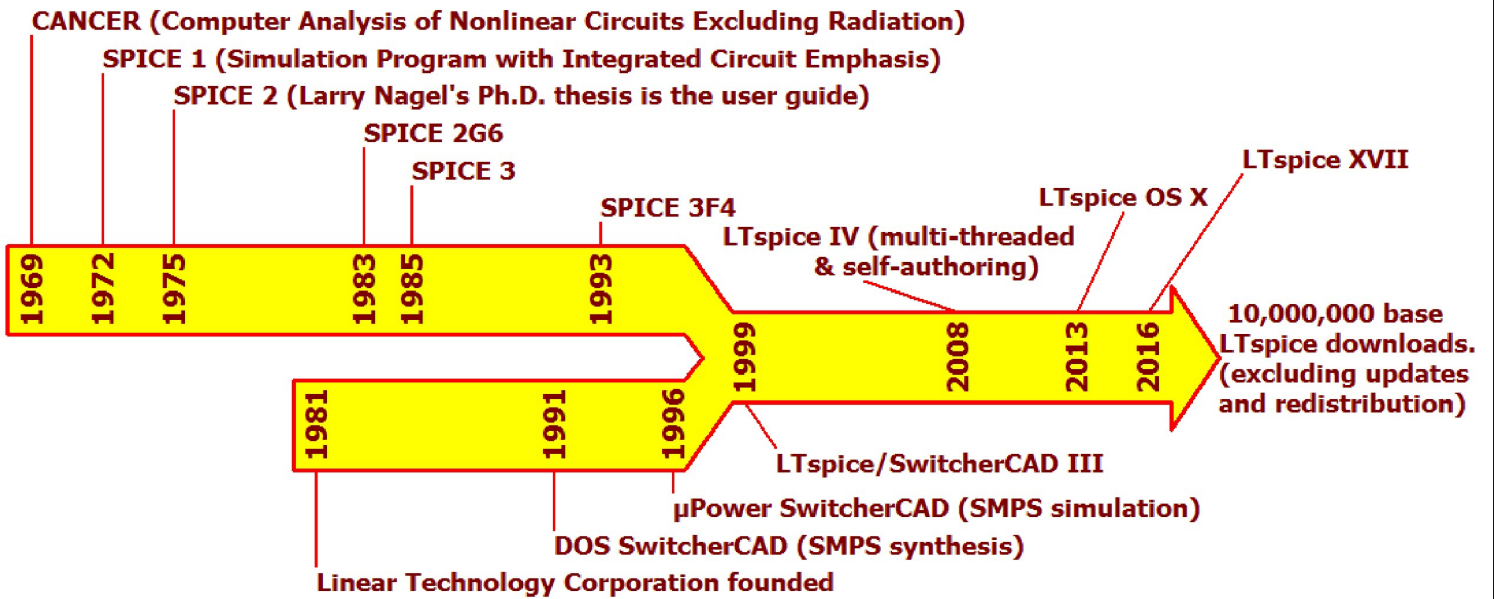
The Best Simulators are Developed by the Concerns that Need them.

- Best charged-particle optic simulator: scanning electron microscope company
- Best MOSFET circuit solver: Intel
- Best radar return solver: Government Intelligence
- Best analog circuit solver: IC company, Linear Technology Corporation

Software companies can't compete because it isn't possible to recoup the NRE with licensing fees. For example, PSpice grosses a few million dollars a year, but LTspice is used in the design and sale of about a billion dollars worth of IC's.



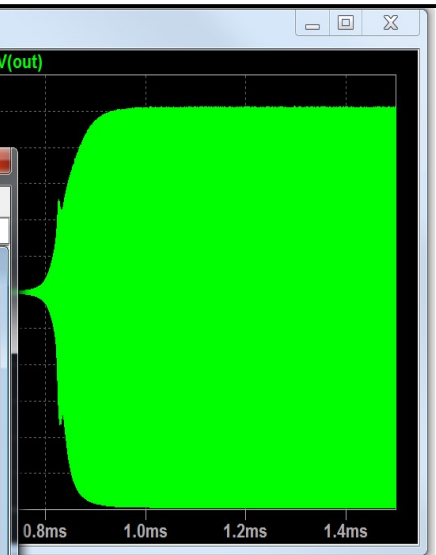
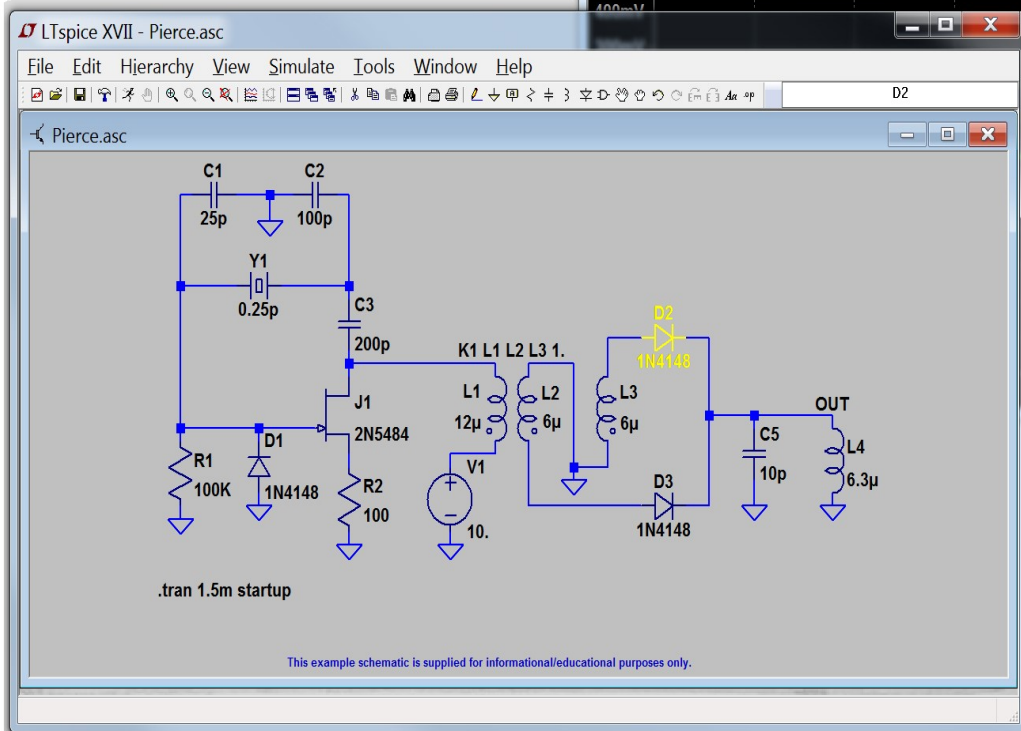
Time Line of SPICE



- LTspice has been the industry de facto standard since mid 2000's
- Downloaded 4 times per minute(excluding updates)
- Distributed 100's of times more than any other SPICE program




LTspice XVII



- Multi-monitor
- x64
- UNICODE

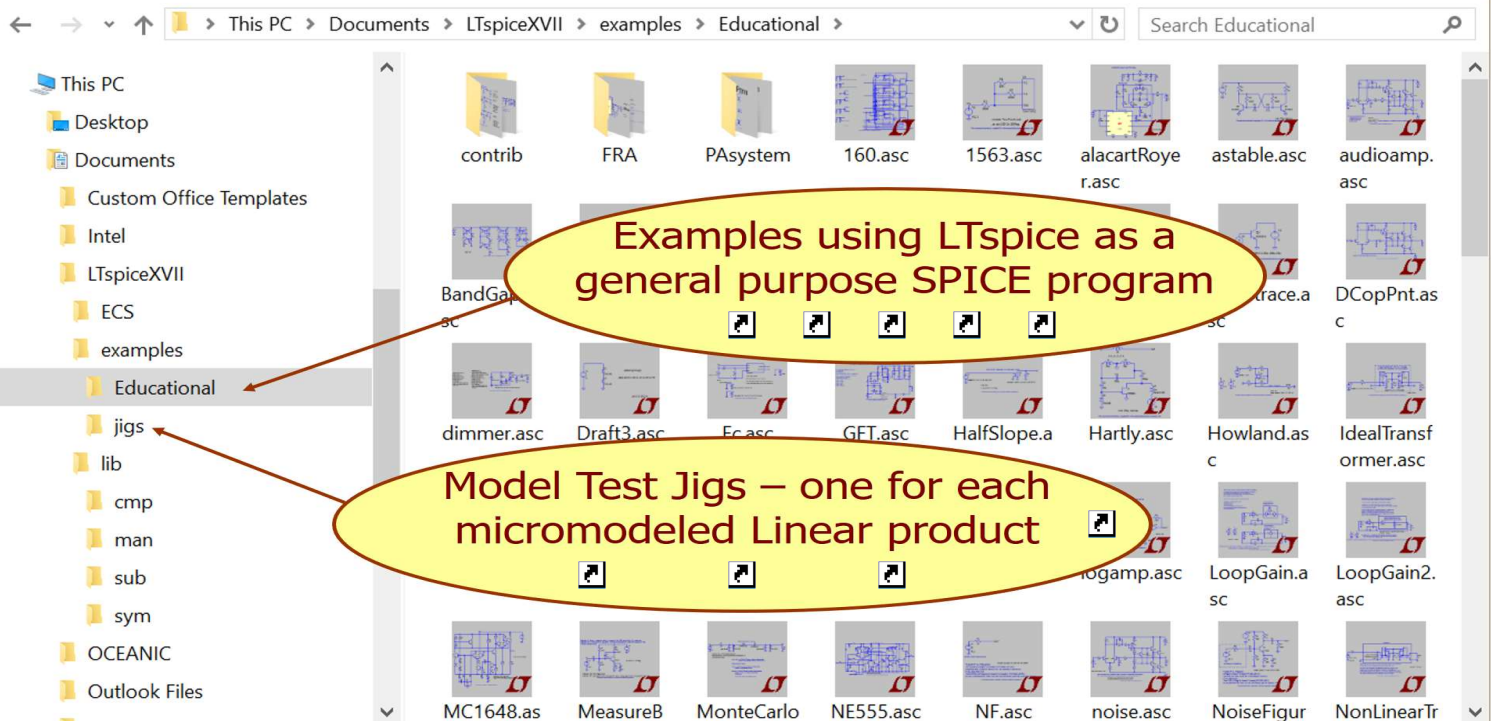


Drafting Your Own Circuits

- General Purpose Schematic Capture
 - Unlimited schematic size
 - Unlimited depth of hierarchy
 - Bidirectional cross-probing
 - Graphical Symbol editor
 - Complete documentation
- Macromodels of 2500 Analog Devices Products
- Integration with Industry Superlative SPICE Simulator
 - Unlimited, professional SPICE proven for IC design
 - Unmatched combination of robustness, accuracy, speed and compatibility
 - Advanced analysis/simulation options, parameter sweeps, FFTs, etc.
 - Use 3rd party models
 - Active independent users' group

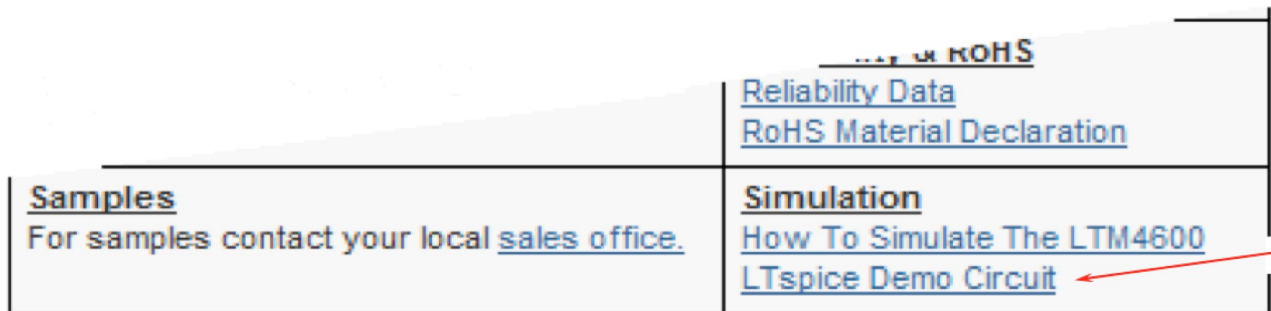


Installation Directory Structure



Additional Resources for Example Files

- <http://www.analog.com>
 - Some products feature an example LTspice schematic












Samples For samples contact your local sales office .	Reliability Data RoHS Material Declaration
	Simulation How To Simulate The LTM4600 LTspice Demo Circuit

- <http://groups.io/g/LTspice> (formerly <http://groups.yahoo.com/group/LTspice>)
- FAE's at Analog
- LTspice@analog.com








Waveform Display Features

- Plot expressions of data assisted with cross probing 
 - Cross probe voltages, device and port currents
 - Differential crossprobing
 - Dissipation expression composed by the schematic
 - Current in a "wire"
 - Dimensional analysis 
 - Horizontal panning with the mouse tilt
- Waveform average and RMS calculator
- Fourier analysis (both .four statements and FFT's) 
- Dynamic waveform data compression 
- Multiple plot planes
 - Attached cursors ganged across plot panes 
- Eye diagrams  
- Complex data: Bode, Nyquist, and Cartesian 
- Parametric plotting (X-Y plotting) 




What Usually Is Modeled?

- Typical performance at room temperature
- Error amp
 - G_m
 - Source/Sink Current
- Oscillator
 - Frequency
 - Duty Cycle Limits
- Switch logic
- Switch current limit
- Switch beta 
- Peak current vs error voltage 
- Slope compensation
- Burst Mode 
- Switch minimum on time
- Pulse skipping 
- PLL capture & phase lock 



What Usually Is Not Modeled?

- Production scatter
- Behavior over temperature
- Catastrophic failure modes 
- Strategic simplification: Oscillator SYNC pin(unless the device has a PLL)
- Tactical simplifications mentioned on the symbol



What Can't Be Counted on to Be Modeled or Not?

- I_q in all modes
- Misc features in shutdown

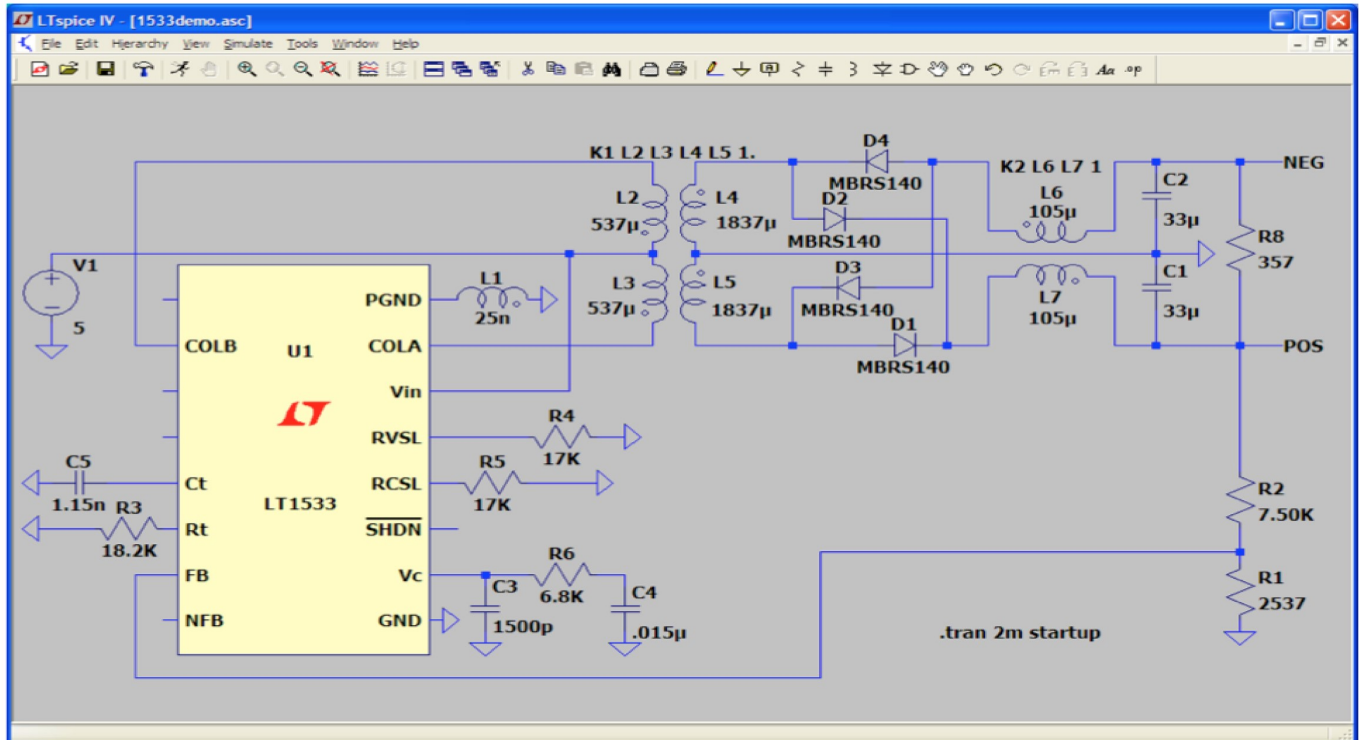


LT1533 Case Study

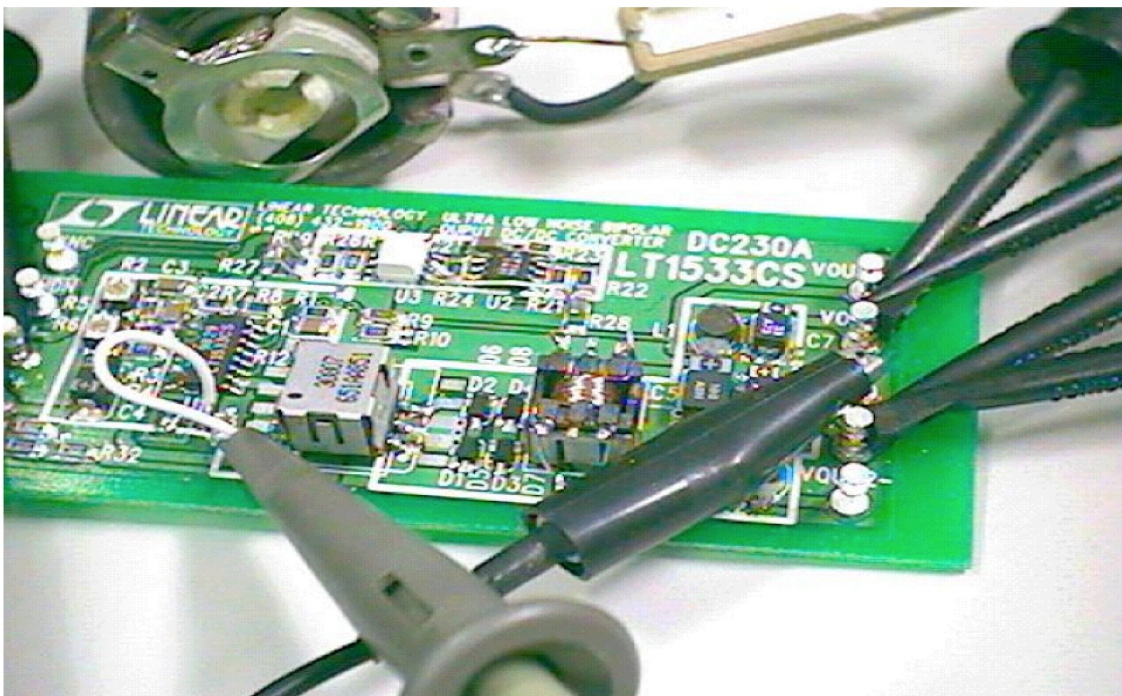
- Voltage and current slew rate limiting
- Complex control logic
- External timing capacitor
- Timing-cap current look-up table
- Demo board available
- Difficult to get efficiency analytically

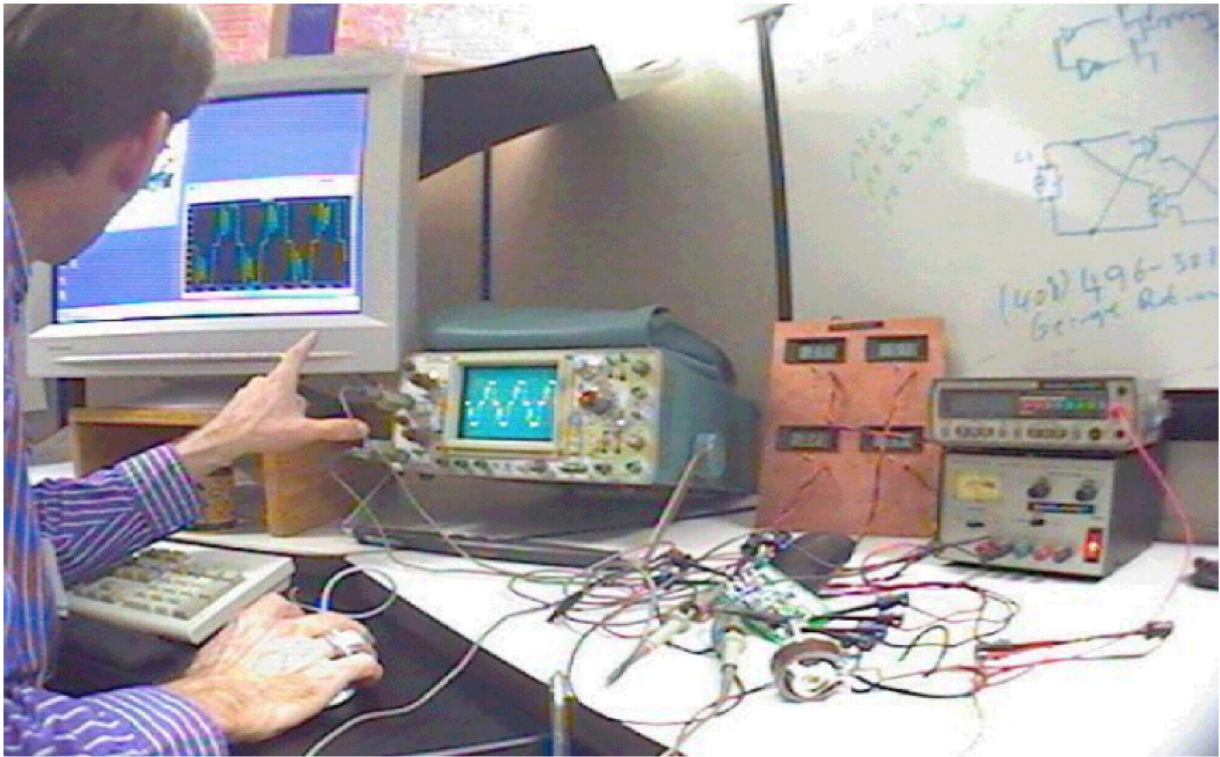


Demo Board Schematic



Demo Board

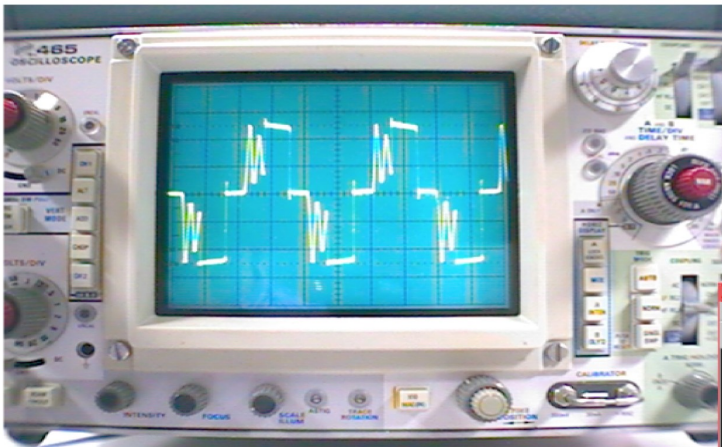




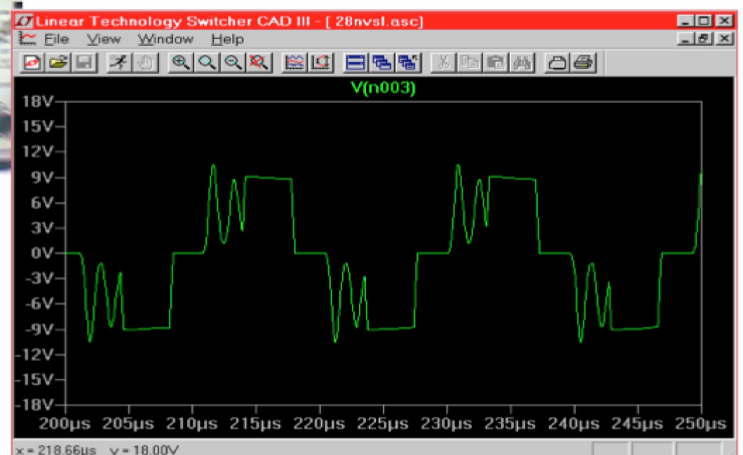
 ANALOG
DEVICES



Minimum Slew Limits



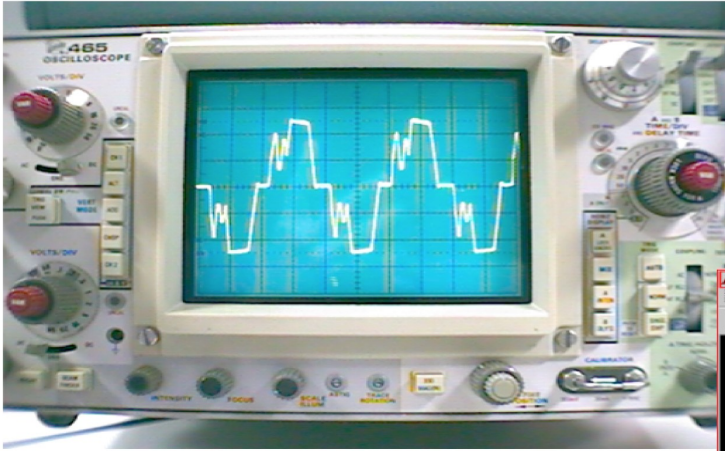
$V_{in} = 5V$
 $V_{out} = +/-5V$
 $I_{out} = 28mA$



 ANALOG
DEVICES



With Voltage Slew Limit



$V_{in} = 5V$
 $V_{out} = \pm 5V$
 $I_{out} = 28mA$



LT1533 Efficiency Comparison

	LTspice	Demo Board
Min. Slew Rate Limit	73.0%	73.0%
With Current Slew Limit	66.0%	65.4%
With Voltage Slew Limit	63.0%	62.0%





SMPS Stability *or* Open Loop Response From the Closed Loop System

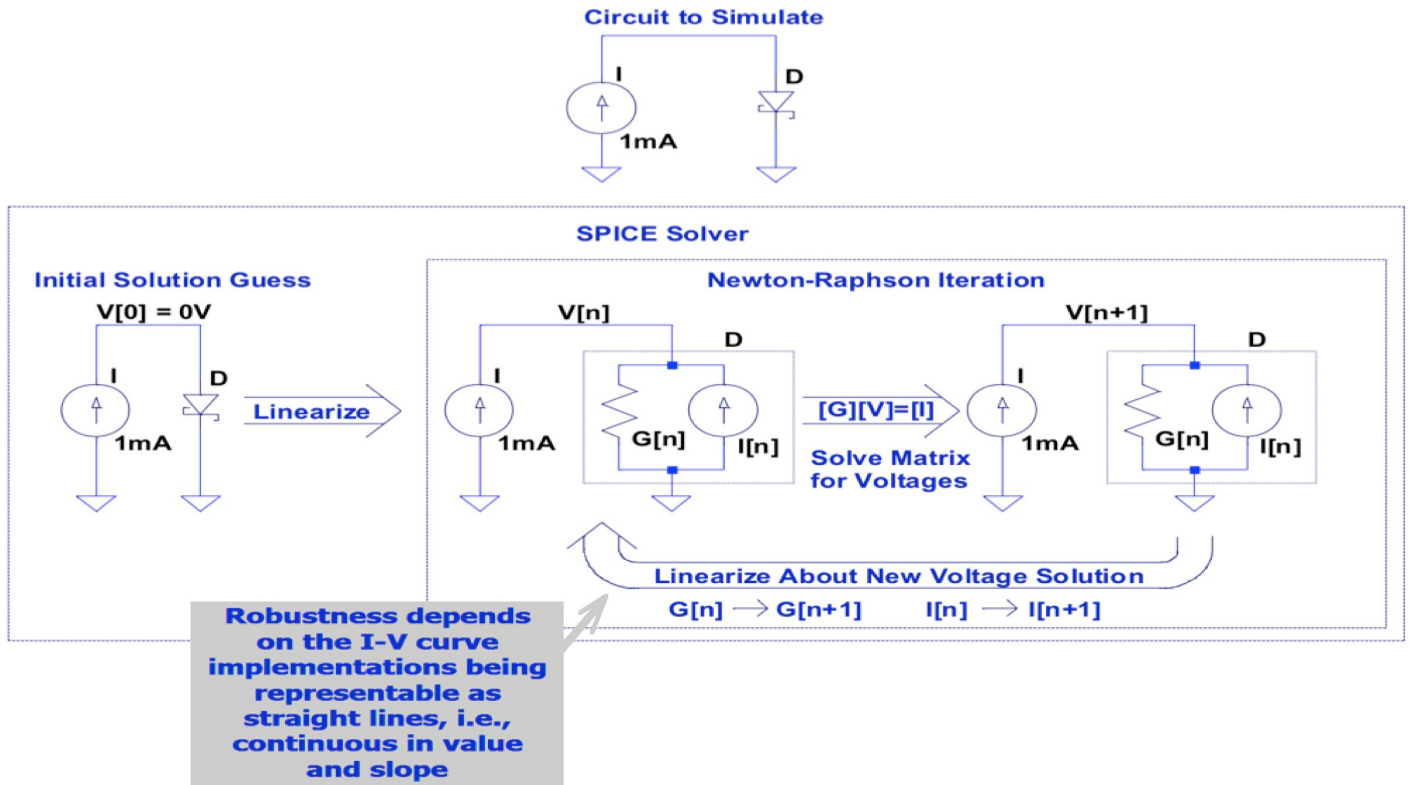


Three Numerical Methods Account for the Success of SPICE

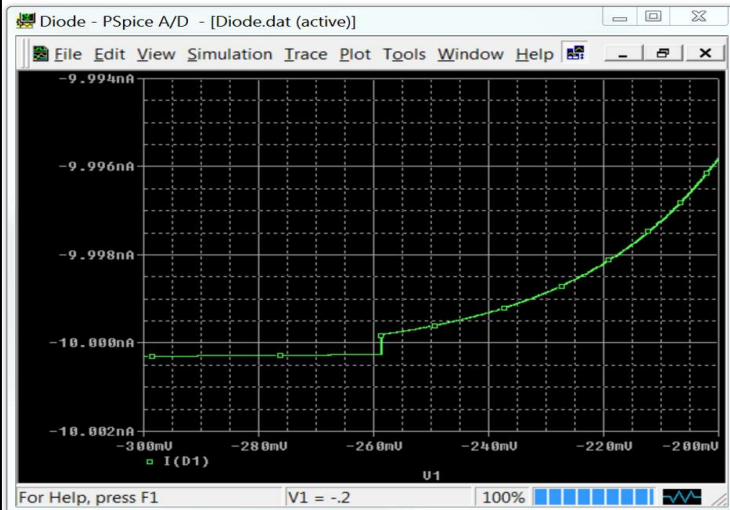
- Newton iteration
- Sparse matrix methods
- Implicit integration



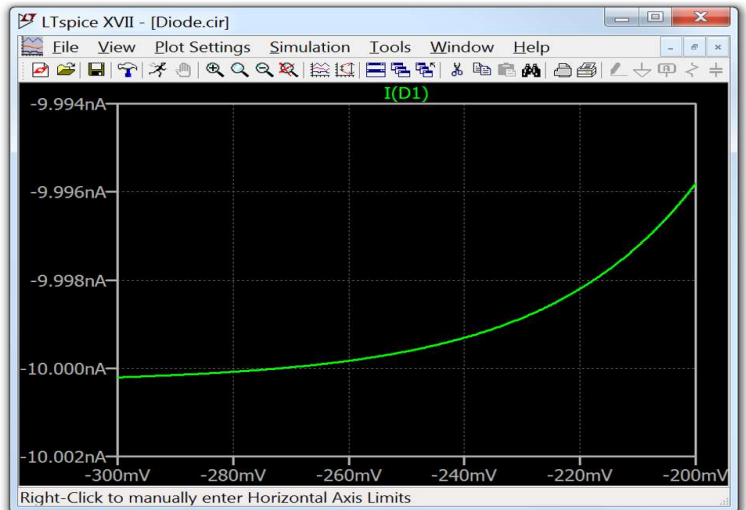
Newton Iteration



Berkeley Diode Discontinuity



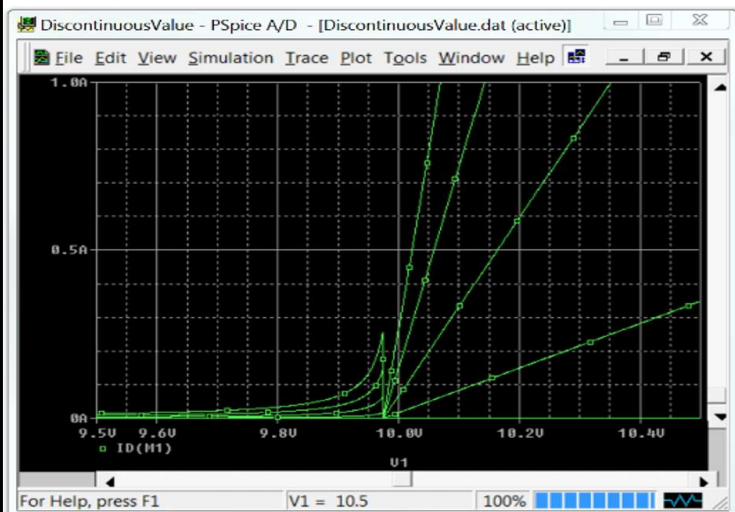
PSpice



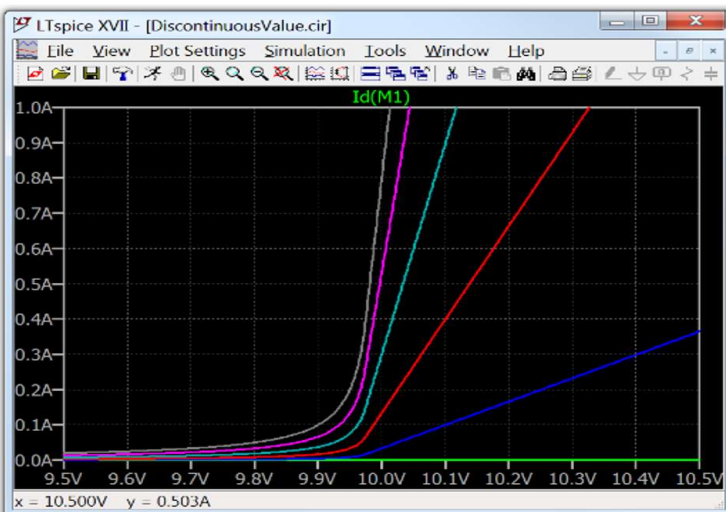
LTspice



Berkeley MOS Discontinuous Value



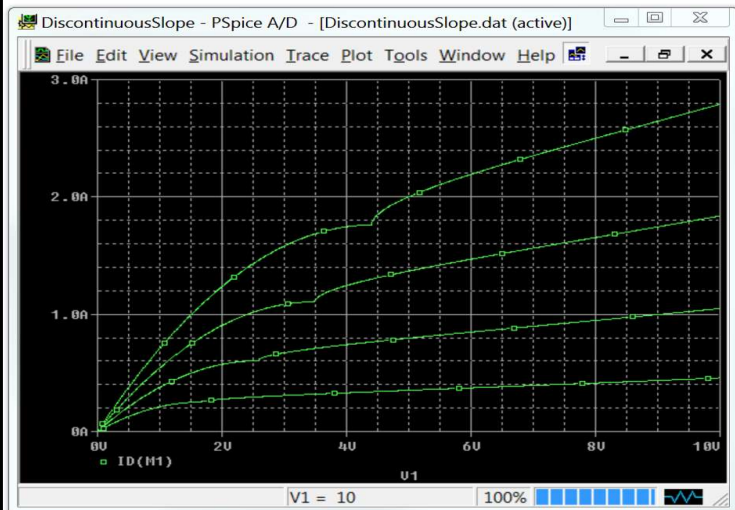
PSpice



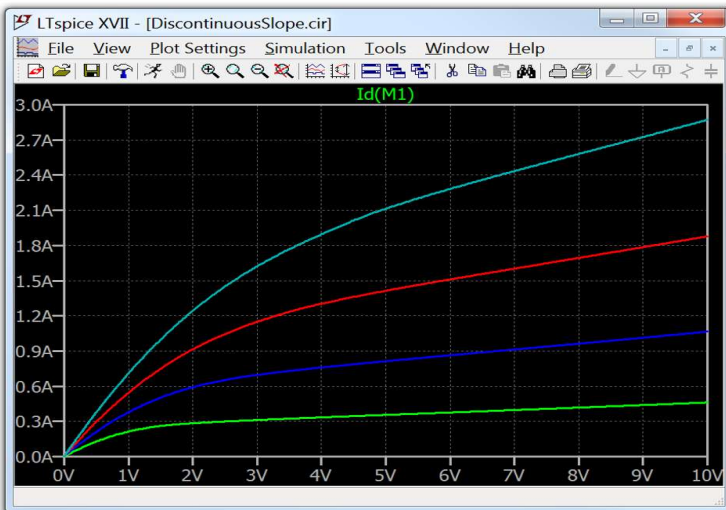
LTspice



Berkeley MOS Discontinuous Slope



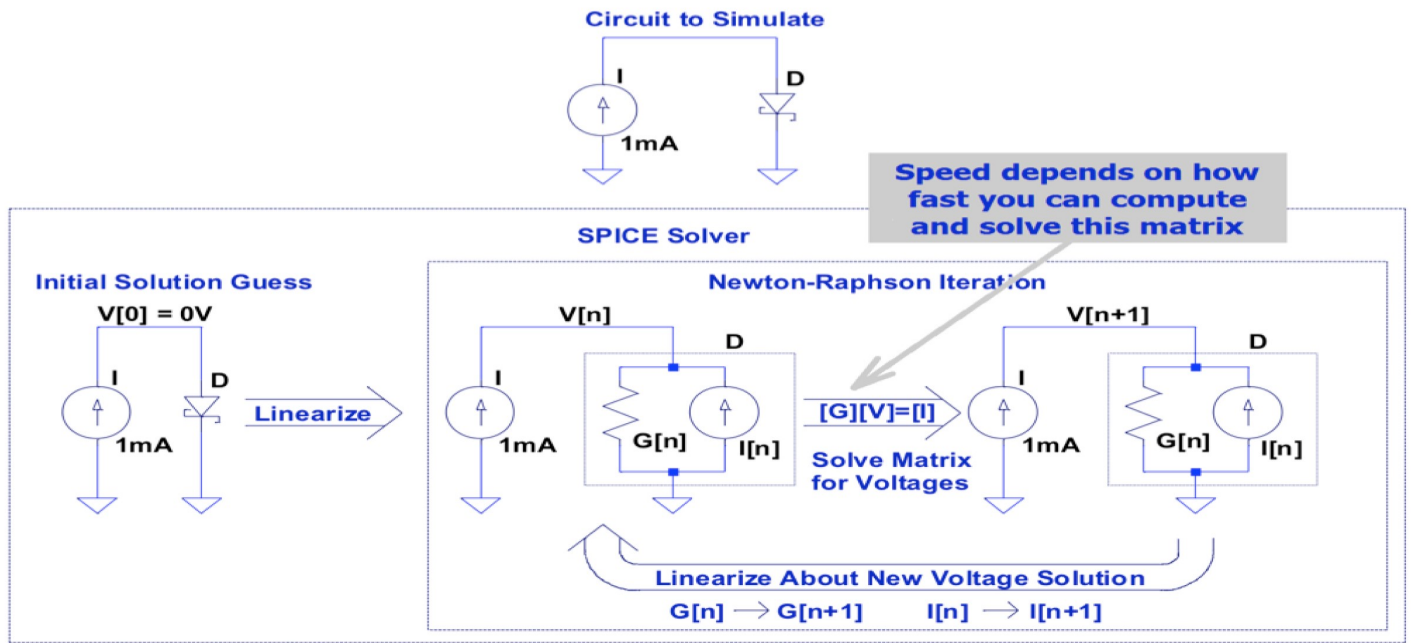
PSpice



LTspice



Newton Iteration



Simulation Speed Determined by

1. Time to Compute the Matrix
2. Time to Solve the Matrix



Simulation Speed Determined by

$O(N)$:

**"Compute the matrix"
means computing
these coefficients**

LTspice's multi-threaded solver computes these coefficients in parallel.

$$\begin{bmatrix} G_{11} & G_{12} & \cdots & G_{1n} \\ G_{21} & G_{22} & & \\ \vdots & & \ddots & \\ \vdots & & & G_{nn} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \end{bmatrix}$$

$O(N^2)$:

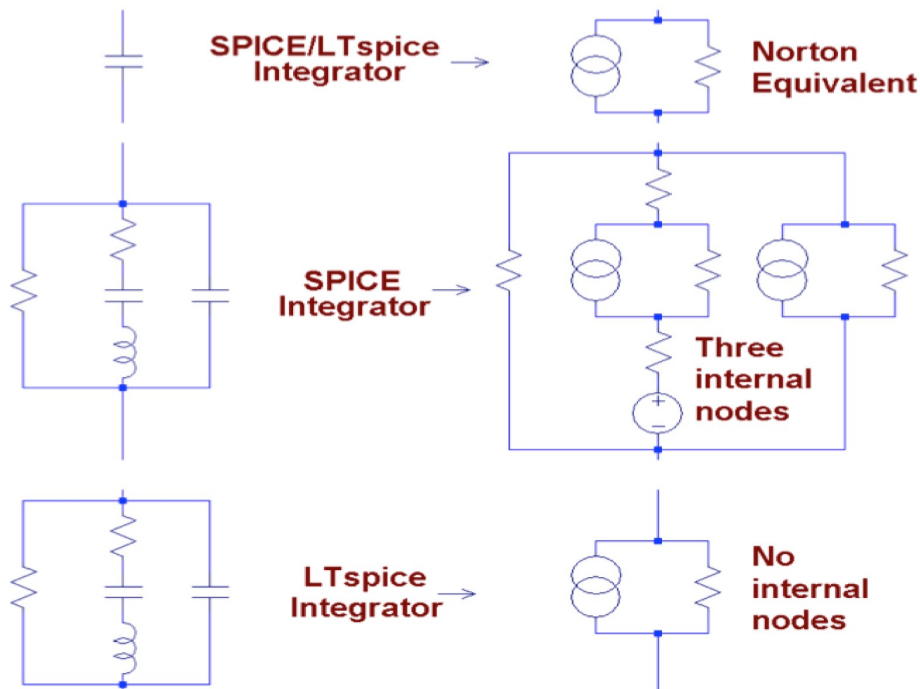
**"Solve the matrix"
means solving for
this vector**

LTspice's self-authoring solver allows the matrix be solved at the theoretical FLOP limit

So use smaller matrices!



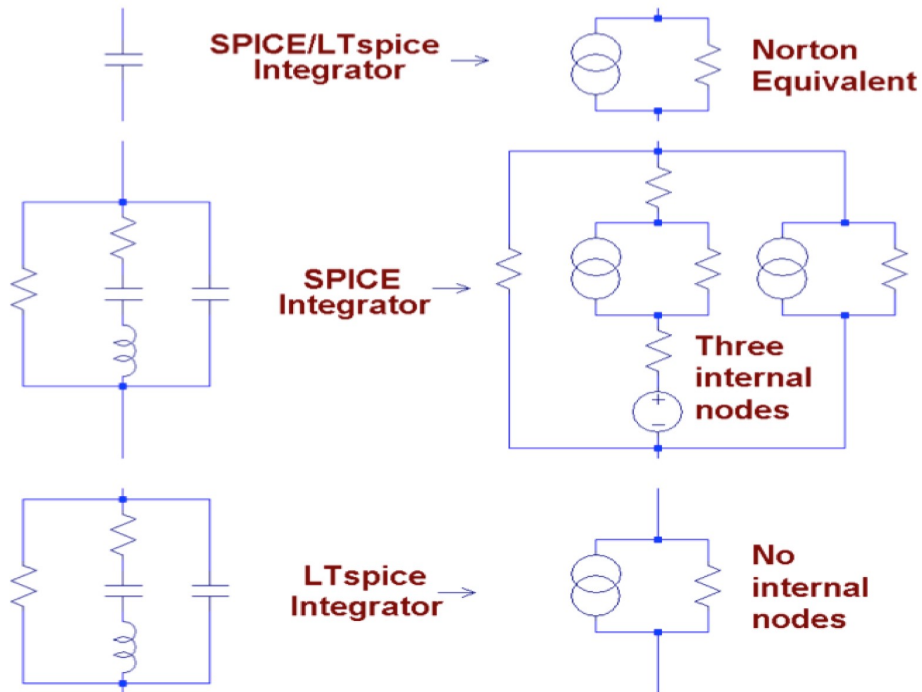
Matrix Node Reduction



But what happens to the accuracy?



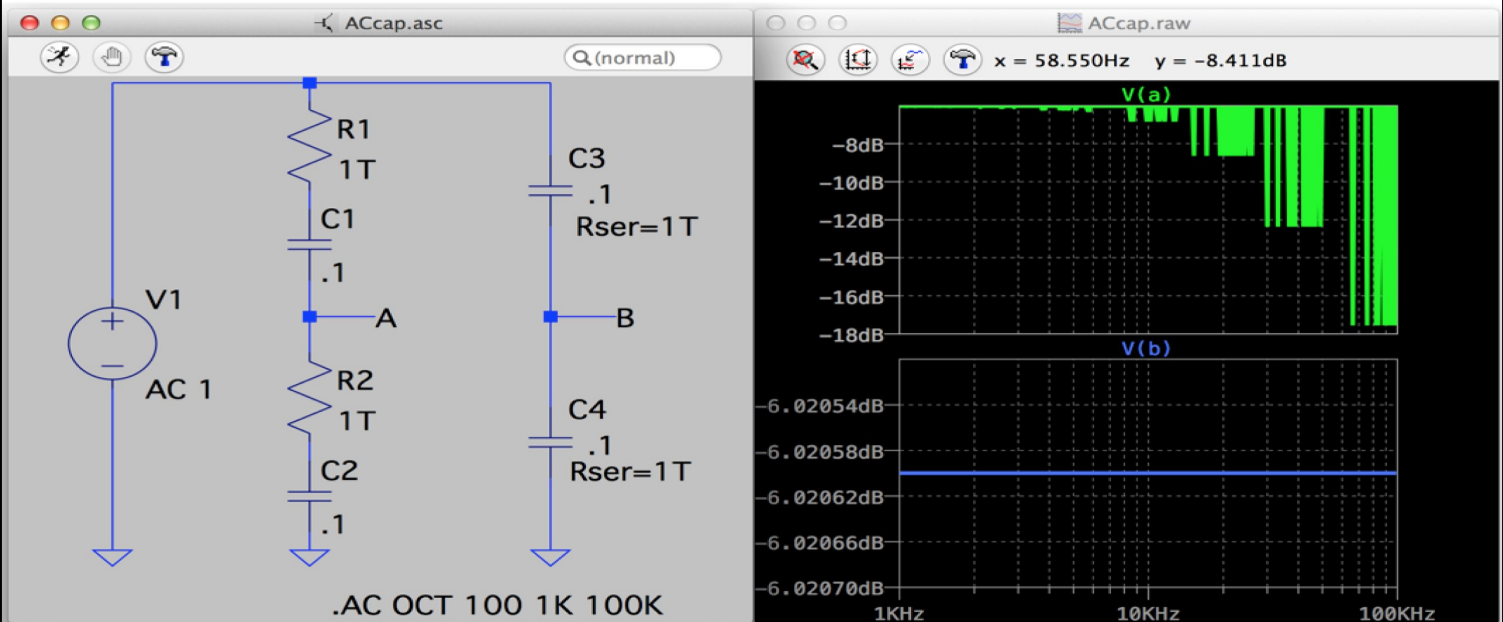
Matrix Node Reduction



Node reduction improves accuracy!



Node Reduction Example



Node reduction improves both speed and accuracy



Implicit Integration

- Circuit reactances give rise to differential equations that are numerically integrated.
- Because the solution looks like $\exp(-\text{const} \cdot \text{time})$, if a normal method; e.g., Euler is used; the error would exponentially deviate from the correct solution and diverge to infinity.
- Implicit methods; e.g., backward Euler; are used in circuit simulation to avoid the singularity. Unfortunately backward Euler is extremely slow and inaccurate, so 2nd order methods are used.

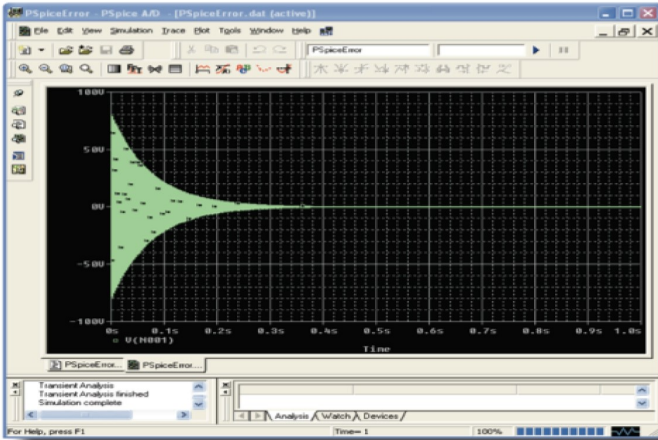
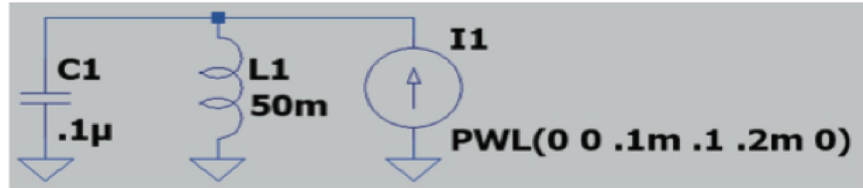


2nd Order Implicit Integration Methods

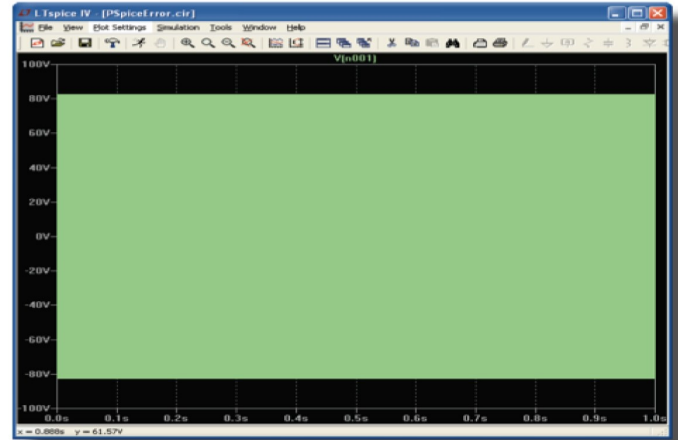
- Trapezoidal(trap)
 - Potential for Ringing artifact
 - Fast
 - Accurate
- Gear
 - No Ringing artifact
 - Slow
 - Inaccurate
- Modified Trap(proprietary to LTspice)
 - No Ringing artifact
 - Fast
 - Most accurate method known



Gear Integration Error



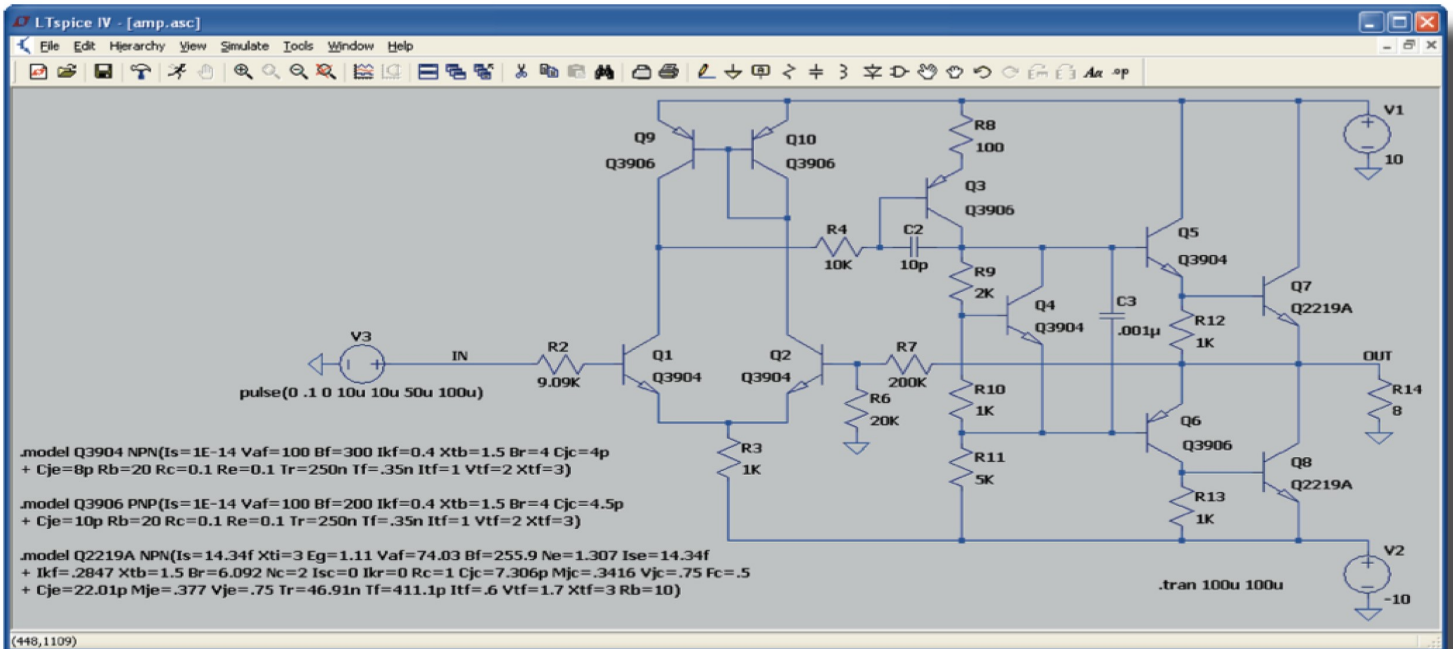
PSpice



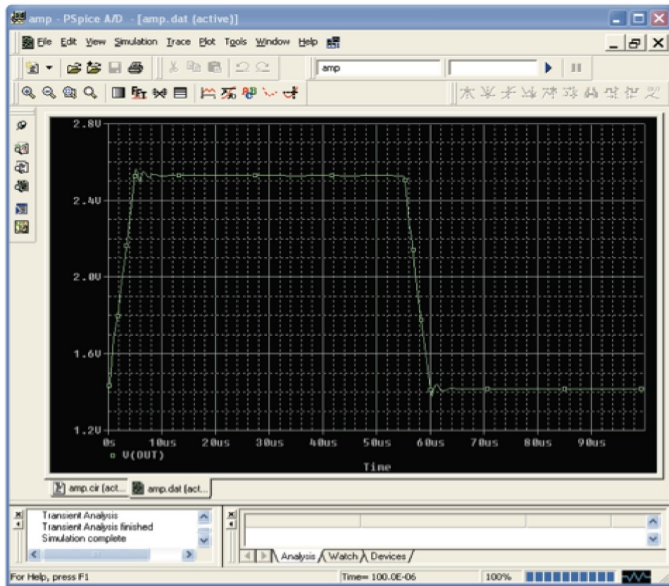
LTspice



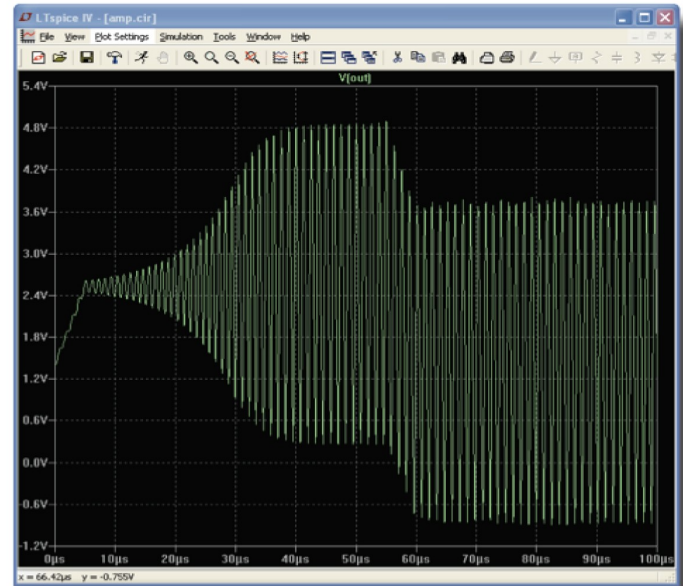
Gear Integration Error In Context of a Practical Example



Gear Integration Error In Context of a Practical Example



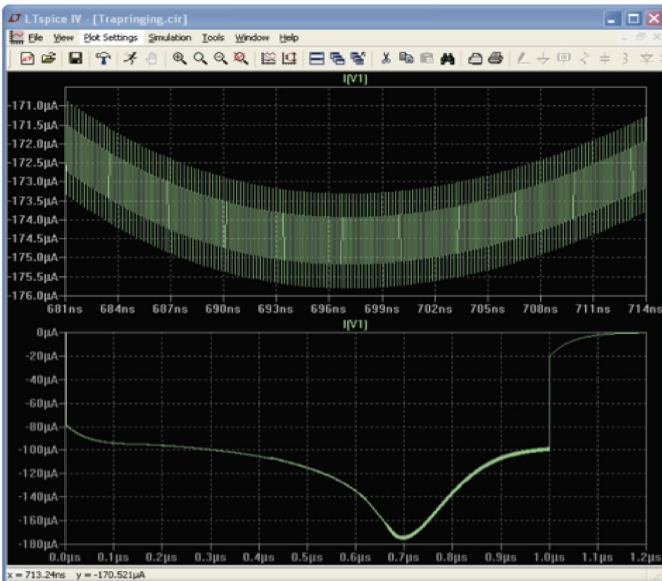
PSpice



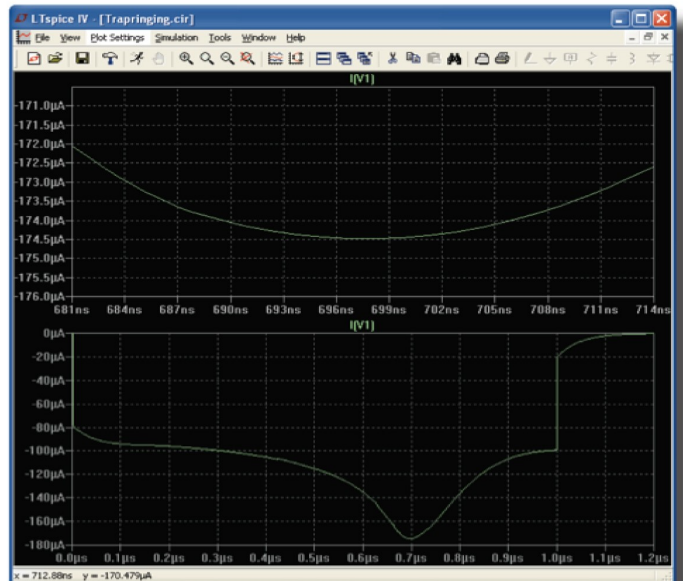
LTspice



Trap Integration Artifact



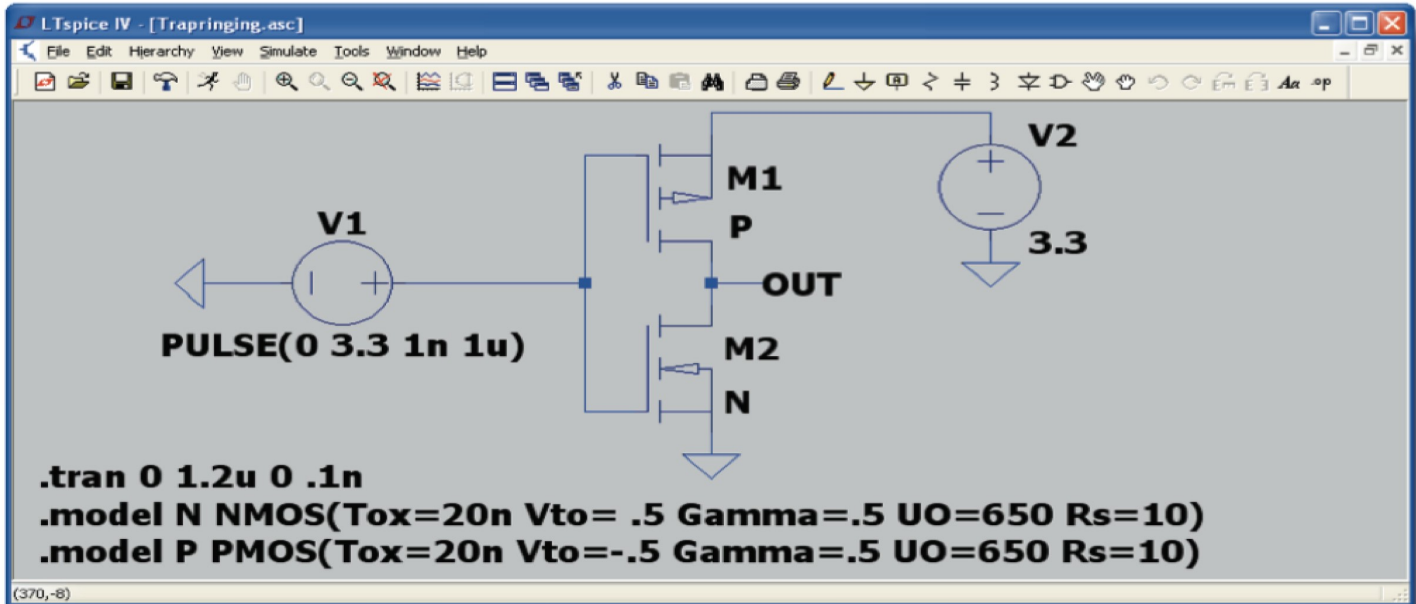
Trap



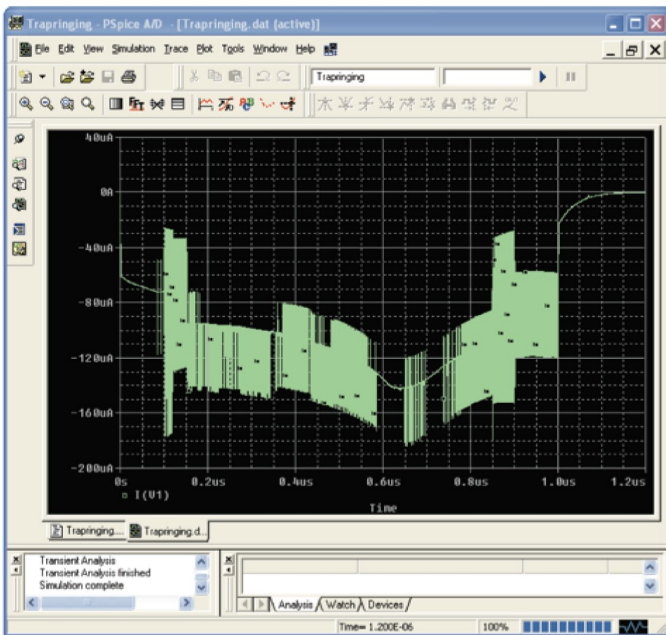
Modified Trap



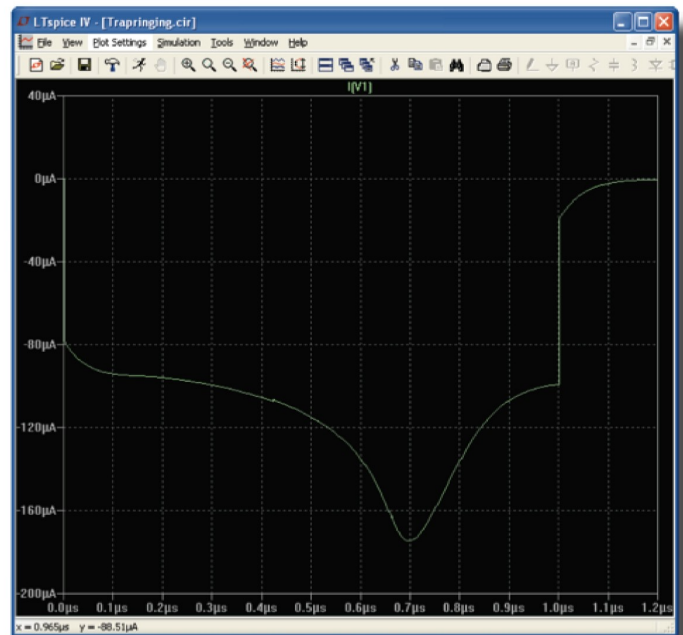
Trap Integration Artifact Circuit



Trap Integration Artifact Circuit






PSpice



LTspice



Three Numerical Methods Account for the Success of SPICE






- Newton iteration
 - Need I-V curves continuous in value and slope Robustness
- Sparse matrix methods
 - Node reduction for speed and accuracy
 - Compute matrix coefficients in parallel threads
 - Solve matrix with self-authoring code Speed
- Implicit integration
 - Proprietary modified trap
 - speed and accuracy of trap
 - No trap ringing Integrity



LTspice was not the first SPICE implementation, nor is it the only free SPICE, but it is the best and most widely used SPICE implementation.

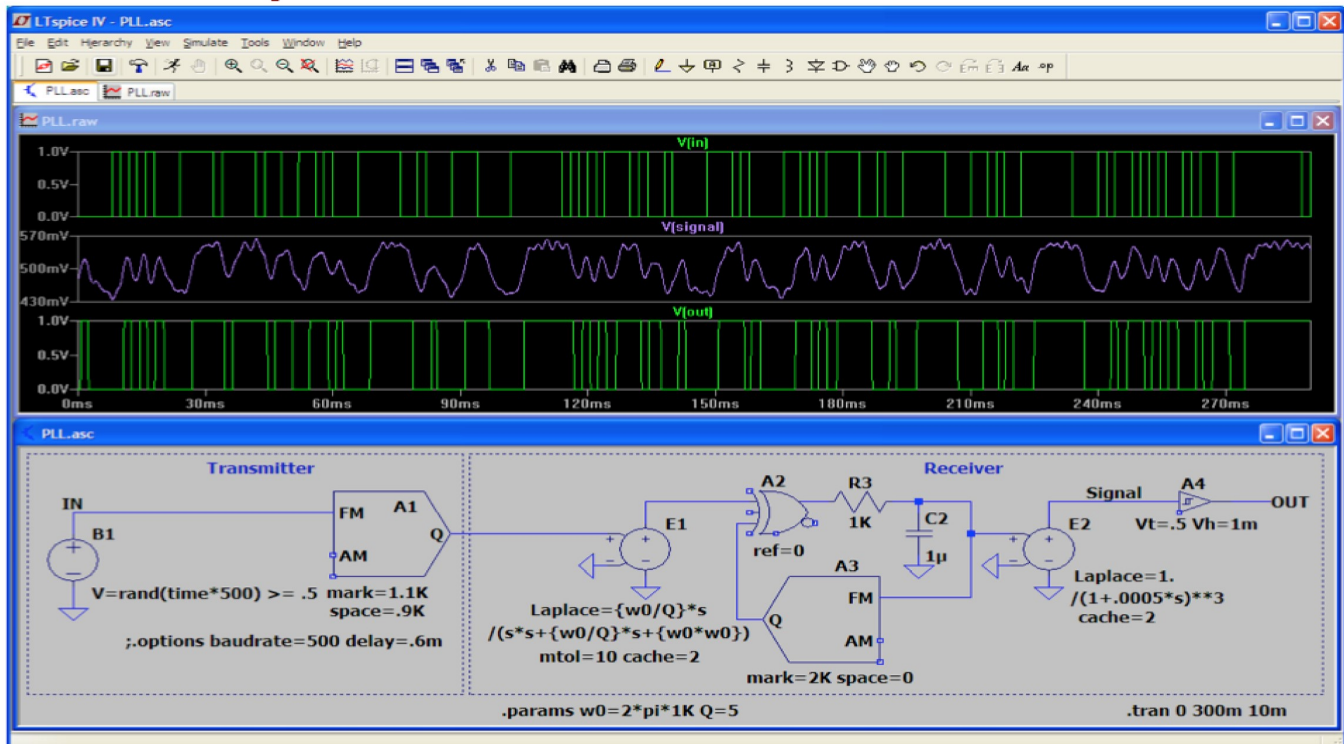


LTspice Behavioral Simulator

- PSPICE style behavioral modeling 
 - Legacy POLY() statements
 - Arbitrary expressions
 - Laplace
 - Look-up tables.
- Arbitrary capacitance: write an expression for the charge. 
- Arbitrary inductor: write an expression for the flux. 
- An original mixed-mode simulator -- not xspice based. 
- Co-simulation for very complex models 



Example Mixed-Mode Simulation

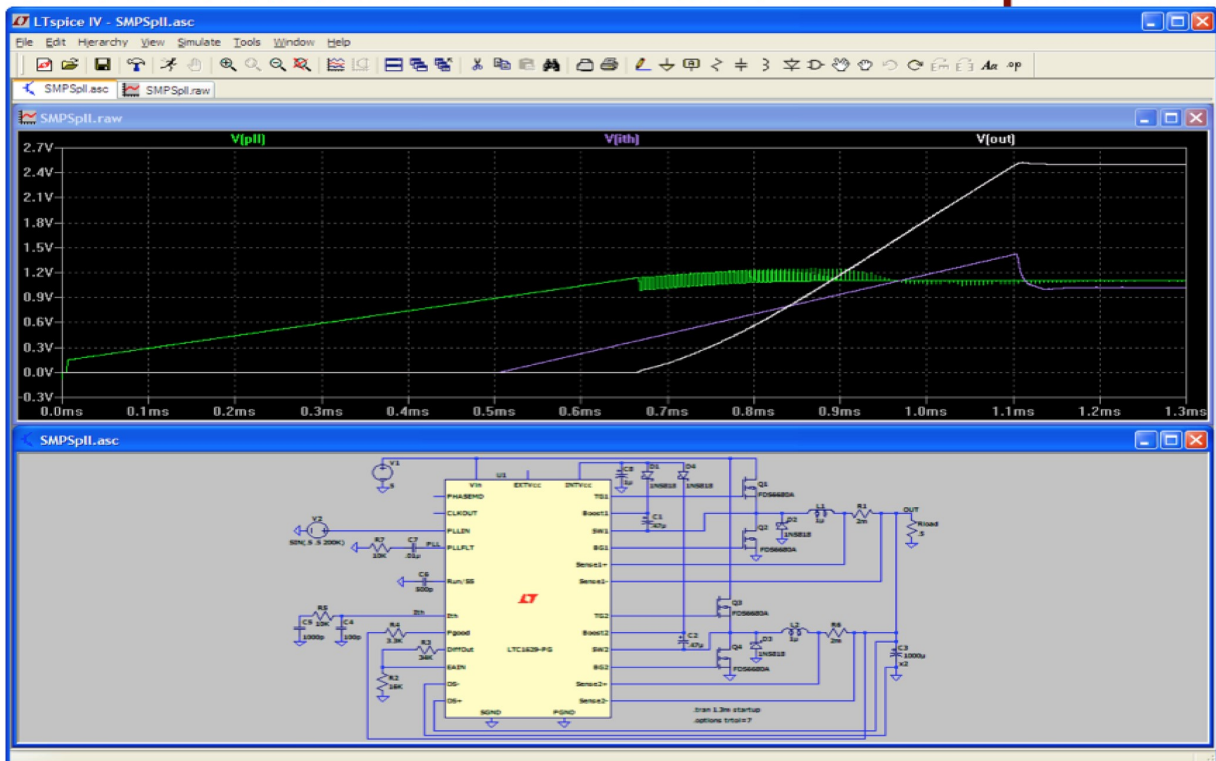


Mixed-Mode Simulator

- Computationally lightweight
- Tight feedback between analog and digital circuitry
 - Implemented as a mix of intrinsic SPICE devices and ~30 optimizing HDL compilers.
 - Predictors aid timestep control.
- Easy to program so that models for new products are usually quick to be generated.



Two-Phase SMPS & PLL Capture



Total elapsed time: 5.508 seconds.



Chan et al. Nonlinear Magnetics

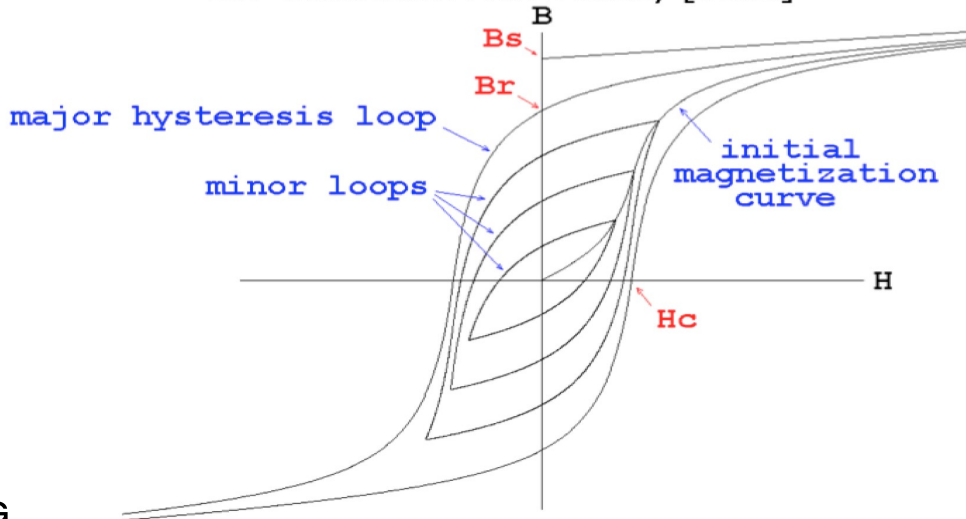
Extended per US Patent 7,502,723

A computationally lightweight model that uses only three parameters to specify the core's major hysteresis loop:

Hc: Coercive force [Amp-turns/meter]

Br: Remnant Flux Density [Tesla]

Bs: Saturation Flux Density [Tesla]

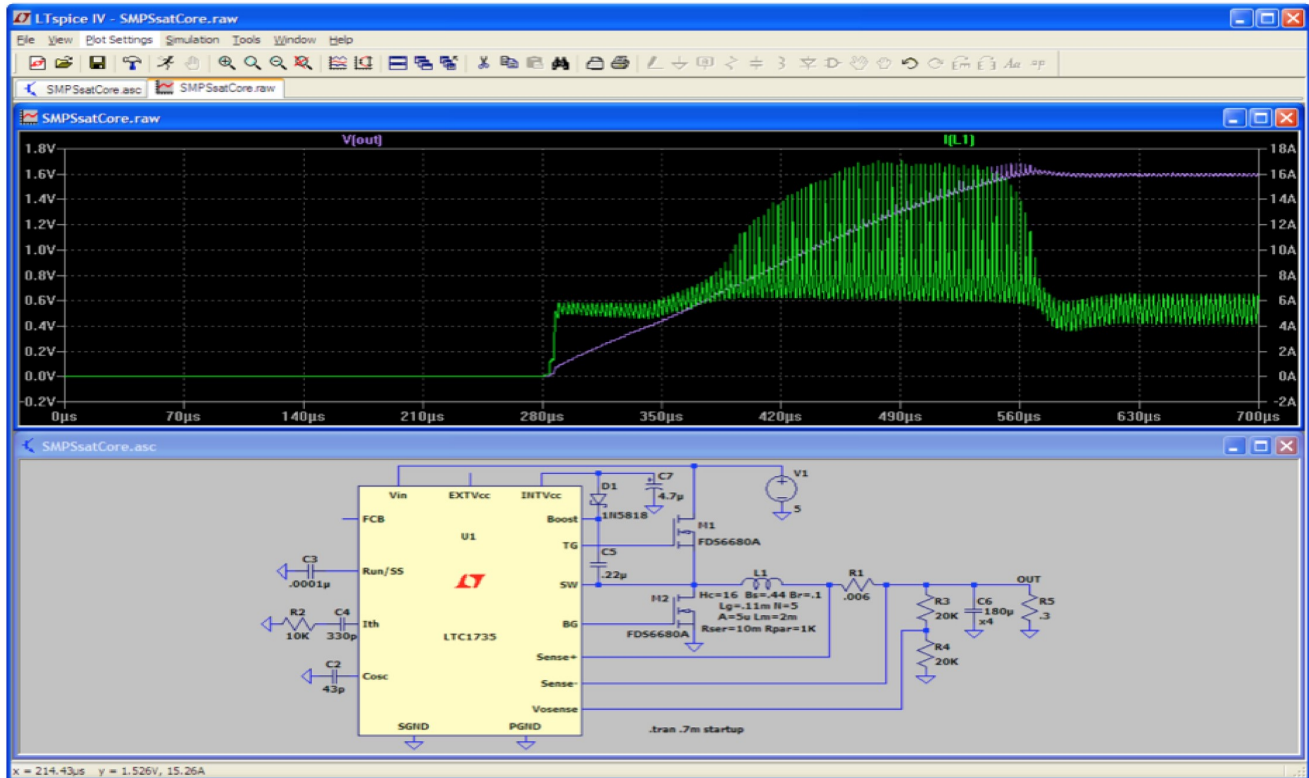


Gapped Core Magnetic Solver

- Core physical dimensions specified with four parameters:
 - Lm: Magnetic Length(excl. gap)[meter]
 - Lg : Length of gap [meter]
 - A: cross sectional area [meter**2]
 - N: number of turns



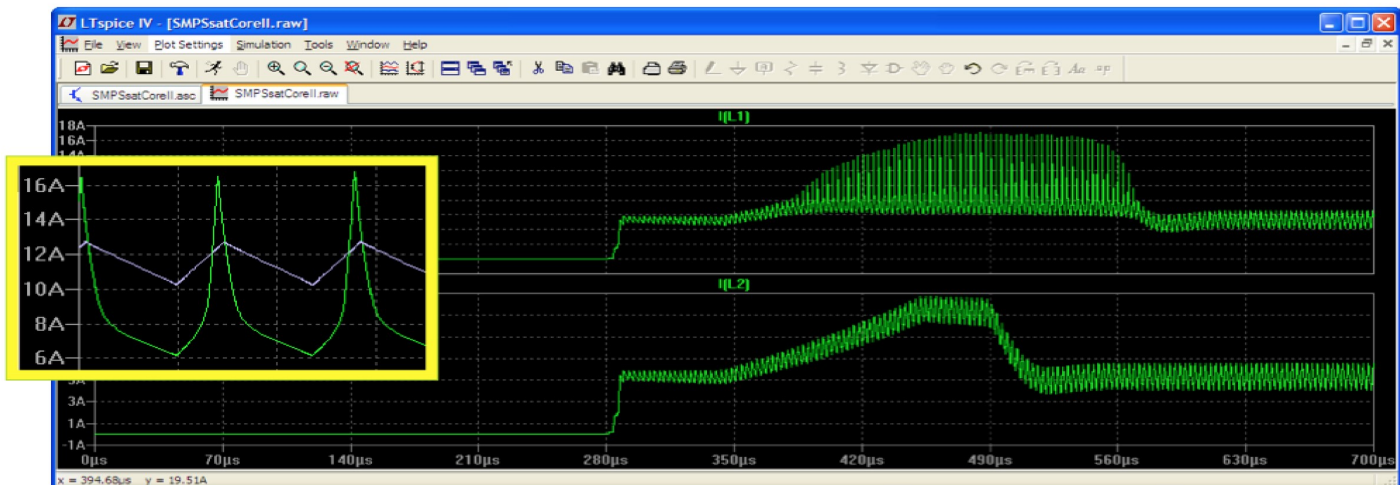
SMPS Inductor Saturation



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Core Saturation Considerations

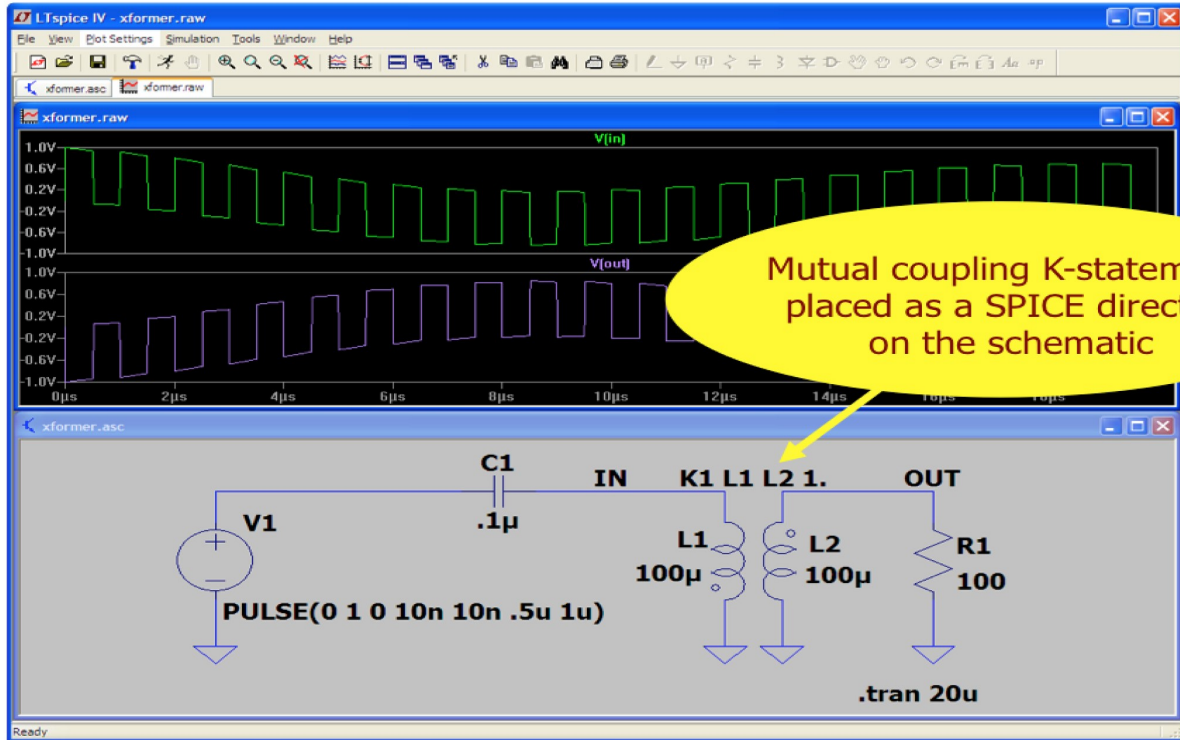
- Saturation flux density goes down monotonically with temperature
- Maximum service temperature plus self-heating
- Controller peak current production scatter
- Startup/transient/short circuit conditions



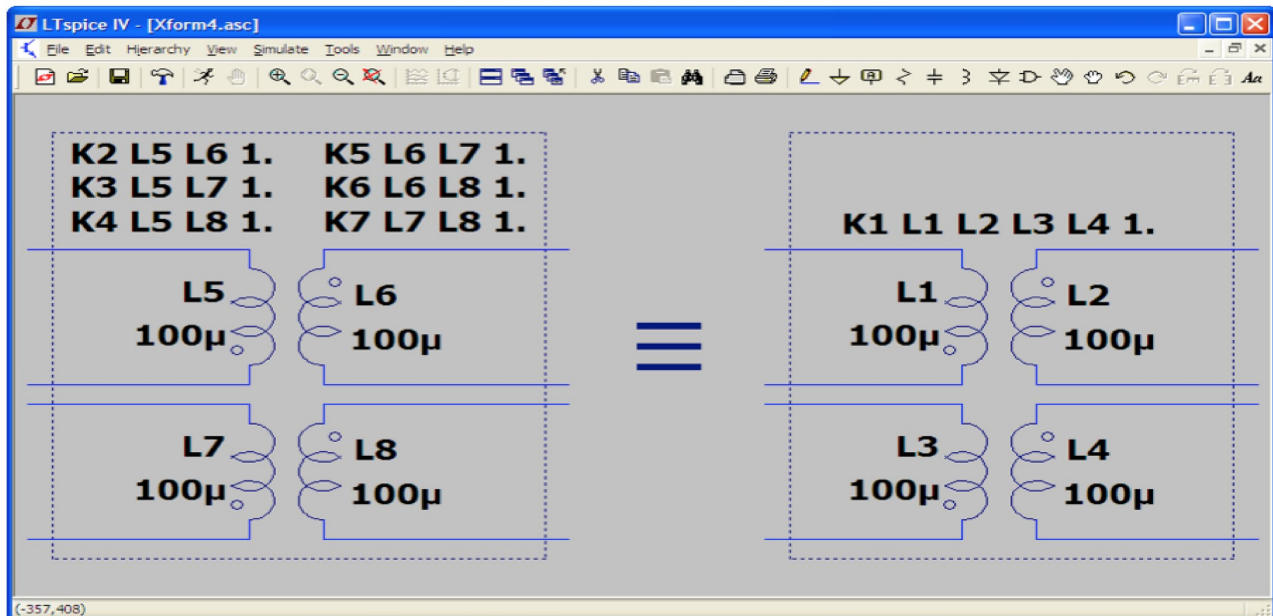
If you use the worst inductor that works in simulation, you will have failures over service temperature and production scatter.

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Simulating Transformers



Multiple Windings



For N windings, the number of mutual couplings is $\frac{N(N-1)}{2}$



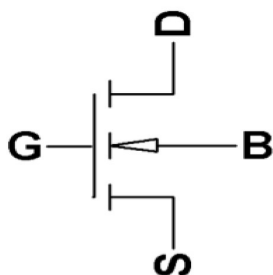
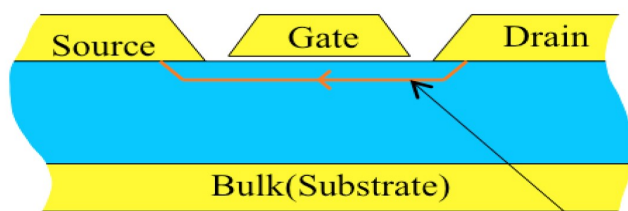
LTspice's Special Enhancements for SMPS Simulation

- Automatic Steady State Detection and Efficiency Computation
- VDMOS MOSFET Model
- Node Reduction
- Mixed-Mode Simulator with intrinsic SMPS controller functions
- Nonlinear magnetics with gapped magnetic circuit solver(US Patent 7,502,723)

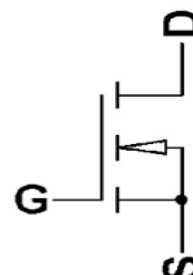
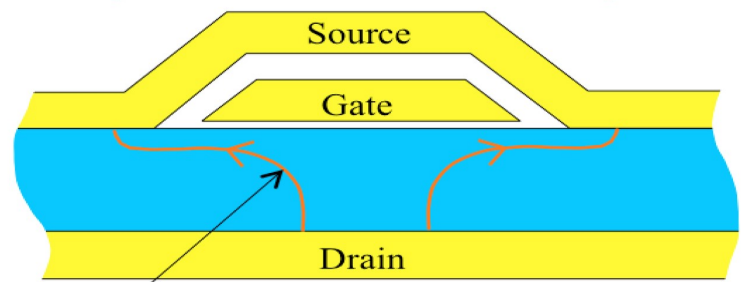


VDMOS MOSFET

Normal Monolithic MOSFET
(Used in IC's)



VDMOS
(Discrete Power MOSFET)

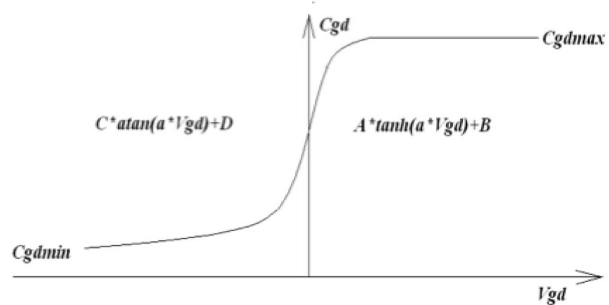
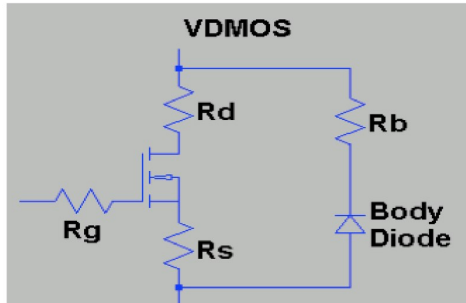


Drain-Source
Current Path

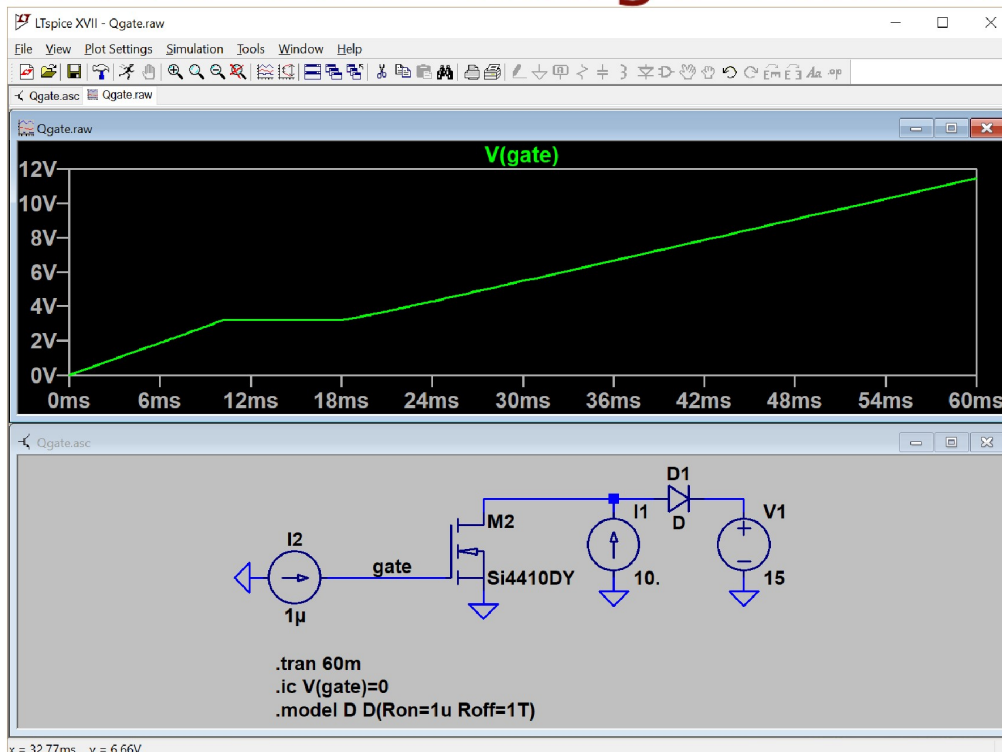


LTC Proprietary VDMOS Model

Replace a problematic subcircuit with a single new intrinsic SPICE device



VDMOS Gate Charge Behavior



And That's Often Not Even the Worst of It!

To get the charge correct: 

The I-V curve got botched: 



How Do I Add 3rd Party Models?

- .model Statements
 - supply parameters for the built-in device equations of native internal devices.
 - Common for diodes, bipolar' s, and JFET' s



- .subckt Statements: Random Librariied Circuitry
 - Automatic symbol generation!






Beware of OpAmp Models

- Boyle Model 
- Noise 













Misc. Advanced Features

- Waveform plot annotations 
- Hierarchy 
 - automatic symbol generation  
- BUS's 
- Fast Access file format  
- .measure statements 
- Optional double precision data files 
- Read/Write .wav files      
- URL's in a .lib and .inc statements 
- Color Preference Editor

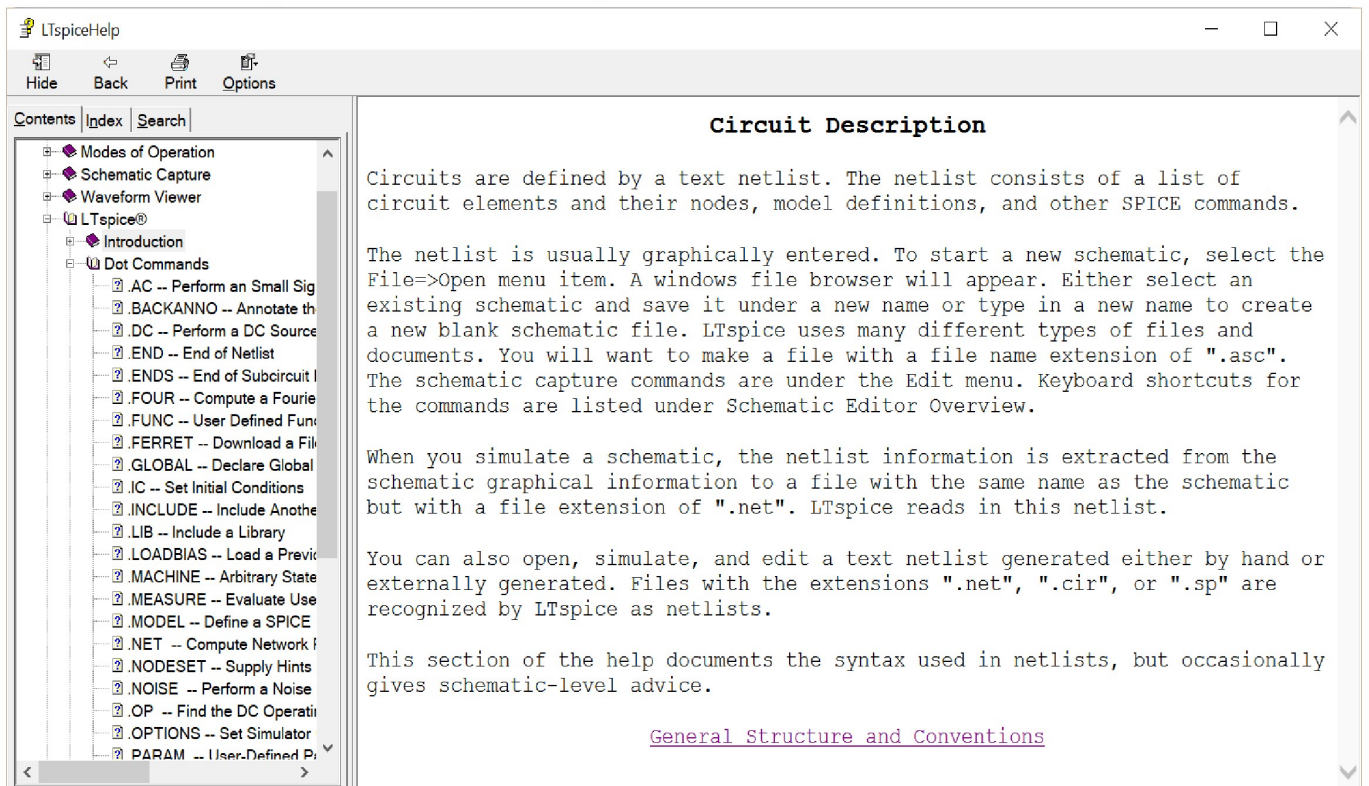


Misc. Advanced Techniques

- User-defined parameters & functions 
- .step'ing a user-defined parameter
 - Overlay simulation runs 
 - Parameter sweeps 
 - Monte Carlo 
 - Optimization 
 - .step'ed .meas data can be plotted   
- Place .op data on the schematic 
- Using the Universal Opamp Model 



Complete Help Documentation



The screenshot shows the LTspiceHelp application window. The title bar reads "LTspiceHelp". Below the title bar is a navigation bar with "Hide", "Back", "Print", and "Options" buttons. The main content area is divided into two panes. The left pane shows a "Contents" tree with the following structure:

- Modes of Operation
- Schematic Capture
- Waveform Viewer
- LTspice®
 - Introduction
 - Dot Commands
 - .AC -- Perform an Small Sig
 - .BACKANNO -- Annotate th
 - .DC -- Perform a DC Source
 - .END -- End of Netlist
 - .ENDS -- End of Subcircuit I
 - .FOUR -- Compute a Fourie
 - .FUNC -- User Defined Func
 - .FERRET -- Download a Fil
 - .GLOBAL -- Declare Global
 - .IC -- Set Initial Conditions
 - .INCLUDE -- Include Anothe
 - .LIB -- Include a Library
 - .LOADBIAS -- Load a Previo
 - .MACHINE -- Arbitrary State
 - .MEASURE -- Evaluate Use
 - .MODEL -- Define a SPICE
 - .NET -- Compute Network I
 - .NODESET -- Supply Hints
 - .NOISE -- Perform a Noise
 - .OP -- Find the DC Operati
 - .OPTIONS -- Set Simulator
 - .PARAM -- User-Defined P

The right pane displays the "Circuit Description" section. The text reads:

Circuit Description

Circuits are defined by a text netlist. The netlist consists of a list of circuit elements and their nodes, model definitions, and other SPICE commands.

The netlist is usually graphically entered. To start a new schematic, select the File=>Open menu item. A windows file browser will appear. Either select an existing schematic and save it under a new name or type in a new name to create a new blank schematic file. LTspice uses many different types of files and documents. You will want to make a file with a file name extension of ".asc". The schematic capture commands are under the Edit menu. Keyboard shortcuts for the commands are listed under Schematic Editor Overview.

When you simulate a schematic, the netlist information is extracted from the schematic graphical information to a file with the same name as the schematic but with a file extension of ".net". LTspice reads in this netlist.

You can also open, simulate, and edit a text netlist generated either by hand or externally generated. Files with the extensions ".net", ".cir", or ".sp" are recognized by LTspice as netlists.

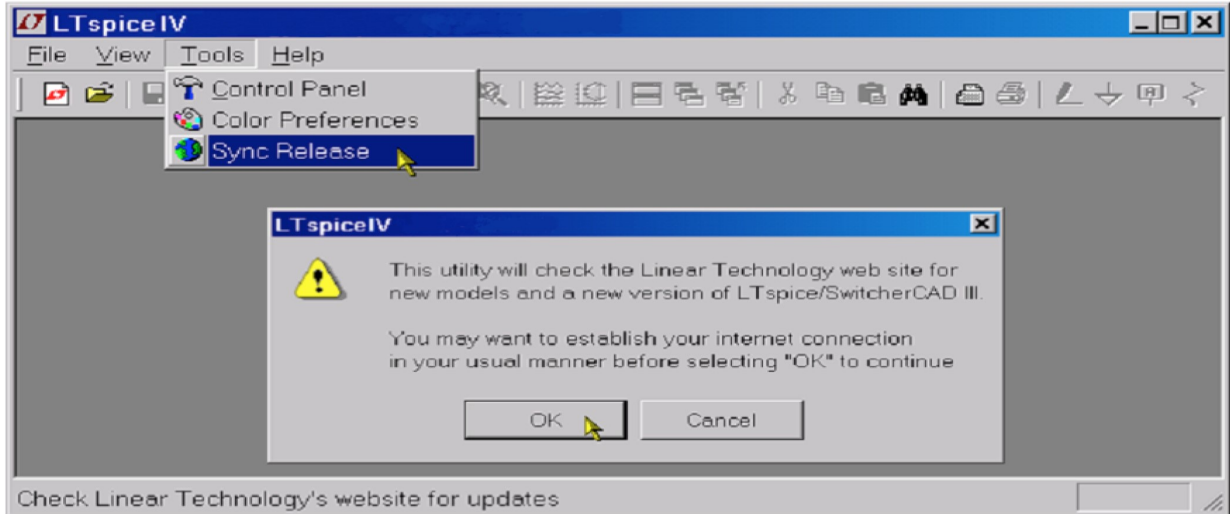
This section of the help documents the syntax used in netlists, but occasionally gives schematic-level advice.

[General Structure and Conventions](#)



Updates With Field Sync

- Incrementally updates your installation off the web
- Automatically merges databases of devices
- Free Lifetime Updates



Thanks for Listening!

